CLAIMS

1. A method including concurrently performing a plurality of memory lookups in response to a sequence of inputs each having information;

each one of said memory lookups being performed in response to a corresponding distinct one of said inputs;

each one of said memory lookups being performed at a corresponding memory;

whereby each one of said sequence of inputs has a memory lookup performed by an associated said memory for at least some of said information.

2. A method as in claim 1, including substantially concurrently providing results responsive to a plurality of said inputs accessing different subsequences of said memories.

3. A method as in claim 1, wherein at least some inputs have their information applied to all said memories at least once, and to at least some of said memories at least twice.

4. A method as in claim 1, wherein each one of said memory lookups is performed in response to a portion of said information.

5. A method as in claim 1, wherein each said input has substantially equal amounts of said information.

6. A method as in claim 1, wherein said memory lookups are each substantially performed on a single monolithic integrated circuit.

7. A method as in claim 1, wherein said sequence of inputs includes at least one of: a destination IP address, an IP address, packet header information.

8. A method as in claim 1, wherein said corresponding memories collectively include lookup results including at least one datum responsive to each one of said inputs.

9. A method as in claim 8, wherein said lookup results collectively include packet forwarding information.

10. A method as in claim 1, wherein said memory lookup includes a sequence of individual memory accesses, each said individual memory access being performed at one of said memories.

11. A method as in claim 10, including substantially concurrently providing results responsive to a plurality of said inputs accessing different subsequences of said memories.

12. A method as in claim 10, wherein at least some inputs have their information applied to all said memories at least once, and to at least some of said memories at least twice.

13. A method as in claim 10, wherein each said input has substantially equal amounts of said information.

14. A method as in claim 10, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory.

15. A method as in claim 10, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory, followed by a second individual memory access at each said memory for at least a subsequence of said memories.

16. A method as in claim 10, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory for only a subsequence of said memories.

17. A method including

coupling each one of a sequence of inputs to a sequence of memories, said sequence having a last memory and a next memory corresponding to each said memory other than said last memory, wherein each said memory is responsive to a distinct portion of said information;

coupling a result from each said memory other than said last memory to its corresponding said next memory in said sequence; and

providing an output of at least one of said memories;

whereby said sequence of inputs is each coupled to said sequence of memories in a pipelined manner to provide said output at a rate substantially equaling one output as each input is received.

18. A method as in claim 17, including substantially concurrently providing results responsive to a plurality of said inputs accessing different subsequences of said memories.

19. A method as in claim 17, wherein at least some inputs have their information applied to all said memories at least once, and to at least some of said memories at least twice.

20. A method as in claim 17, wherein each said input has substantially equal amounts of said information.

21. A method as in claim 17, wherein said sequence of inputs includes at least one of: a destination IP address, an IP address, packet header information.

22. A method as in claim 17, wherein said sequence of memories are substantially included in a single monolithic integrated circuit.

23. A method as in claim 17, wherein said output is responsive to a sequence of individual memory accesses, each said individual memory access being performed at one of said memories.

24. A method as in claim 23, wherein at least some inputs have their information applied to all said memories at least once, and to at least some of said memories at least twice.

25. A method as in claim 23, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory.

26. A method as in claim 23, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory, followed

by a second individual memory access at each said memory for at least a subsequence of said memories.

27. A method as in claim 23, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory for only a subsequence of said memories.

28. A method as in claim 17, wherein said sequence of memories collectively include lookup results including at least one datum responsive to each one of said inputs.

29. A method as in claim 28, wherein said lookup results collectively include a set of packet forwarding information.

30. Apparatus including a circuit integrated onto a monolithic semiconductor chip, said circuit including

a sequence of registers each having a portion of a corresponding lookup search key in a sequence of said lookup search keys, each said register coupled to a corresponding one of a sequence of on-chip memories;

a subsequence of said memories not including a last said memory each having an output register associated therewith, said output register being coupled to an associated next said memory for each said memory in said subsequence;

a plurality of said memories capable of operating substantially concurrently each on a portion of a corresponding plurality of said lookup search keys;

whereby said sequence of registers is capable of coupling each lookup search key in portions to said sequence of memories, each said memory being responsive to each said lookup search key in sequence, each said lookup search key being coupled to each said memory in sequence.

31. Apparatus as in claim 30, including an output register associated with said last memory and coupled to an output of said apparatus.

32. Apparatus as in claim 30, including an output register associated with said last memory, said output register being coupled to an associated earlier memory in said sequence.

33. Apparatus as in claim 30, wherein a plurality of output registers associated with different memories are each coupled to an output for said circuit.

34. Apparatus as in claim 30, wherein an output register associated with a memory other than said last memory is coupled to an output for said circuit.

35. Apparatus as in claim 30, wherein said lookup search key includes at least one of: a destination IP address, an IP address, packet header information.

36. Apparatus as in claim 30, wherein said memories collectively include lookup results including at least one datum responsive to each one of said inputs.

37. Apparatus as in claim 36, wherein said lookup results collectively include packet forwarding information.

38. Apparatus including

a sequence of memories, said sequence having a last memory and a next memory corresponding to each said memory other than said last memory, each said memory being coupled to a distinct portion of one of a sequence of lookup search keys;

each said memory other than said last memory being coupled to its corresponding said next memory in said sequence; and

whereby said sequence of inputs is each coupled to said sequence of memories in a pipelined manner to provide said output at a rate substantially equaling one output as each input is received.

39. Apparatus as in claim 38, wherein a plurality of output registers associated with different memories are each coupled to an output for said circuit.

40. Apparatus as in claim 38, wherein an output register associated with a memory other than said last memory is coupled to an output for said circuit.

41. Apparatus as in claim 38, wherein said last memory is coupled to an associated earlier memory in said sequence.

42. Apparatus as in claim 38, wherein said sequence of lookup search keys includes at least one of: a destination IP address, an IP address, packet header information.

43. Apparatus as in claim 38, wherein said sequence of memories collectively include lookup results including at least one datum responsive to each one of said lookup search keys.

44. Apparatus as in claim 43, wherein said lookup results collectively include a set of packet forwarding information.